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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/505,287	08/19/2004	Willem Jan Toren	FR02 0010 US	5180

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EXAMINER	
CHEN, ERIC BRICE	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 05/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/505,287	TOREN, WILLEM JAN	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *10-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-13* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction is required under 35 U.S.C. 121 and 372.

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1.

In accordance with 37 CFR 1.499, applicant is required, in reply to this action, to elect a single invention to which the claims must be restricted.

Group I, claims 1-9, drawn to a method of forming electrical connections.

Group II, claims 10-12, drawn to an integrated circuit.

Group III, claim 13, drawn to an electrical or electronic device.

2. The inventions listed as Groups I-III do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: Group II requires that the intermediate layer is flush with an edge of the apertures, a feature not claimed in Groups I and II; Group III encompasses an entire electrical device, which includes components other than the integrated circuit.

3. During a telephone conversation with Peter Zawilski on May 16, 2006, a provisional election was made without traverse to prosecute the invention of Group I, claims 1-9. Affirmation of this election must be made by applicant in replying to this Office action. Claims 10-13 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. Claims 1-3 and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Hause et al. (U.S. Patent No. 5,843,625).

7. As to claim 1, Hause discloses a method of forming electrical connections on a substrate (column 1, lines 9-13), comprising the following steps: a) depositing an intermediate layer of material (104/106) on a substrate (100) (column 6, lines 15-41; Figure 2), b) forming an etching mask (108) on the intermediate layer (104/106) (column 6, lines 42-45), said mask (108) having at least one window (column 6, lines 47-49; Figure 3) having dimensions which are larger than the dimensions envisaged for the electrical connections to be realized (column 6, lines 47-49; column 8, lines 36-44), c) etching the intermediate layer of material (104/106) through the window of the mask (108) in order to form therein at least one aperture (110), having lateral side-walls (111) (column 6, lines 55-62), for receiving the electrical connections (column 8, lines 9-11; Figure 8), d) coating the lateral side-walls of the aperture with a spacer (114) in order to

narrow the aperture (column 7, lines 28-33; column 8, lines 36-44), e) depositing at least one conductor material (125) so as to fill the narrowed aperture (column 8, lines 9-11; Figure 8), and f) performing an abrasion operation in order to remove excess conductor material outside the narrowed aperture (column 8, lines 25-31).

8. As to claim 2, Hause discloses that the step a) utilizes a dielectric material for forming the intermediate layer (104/106) (column 6, lines 15-24, lines 37-39) while a metallic conductor material is used in the step e) (column 8, lines 22-23).

9. As to claim 3, Hause discloses that the step d) comprises the deposition of a layer of an insulating coating material (column 7, lines 12-15), followed by the anisotropic etching of this layer so as to preserve a part thereof on the side-walls of the aperture (column 7, lines 19-21; Figure 6).

10. As to claim 7, Hause discloses that apertures are etched which extend right through the intermediate layer (104/106) (Figure 7).

11. As to claim 8, Hause discloses the mask (108) is formed by means of a photolithography technique (column 6, lines 49-53), and in which the narrowed apertures have dimensions (d) which are referred to as "ultimate" dimensions which are smaller than those that can be achieved by means of said photolithography technique (column 8, lines 36-44).

12. As to claim 9, Hause discloses that the electrical connections comprise wiring tracks and/or terminals and/or vias between layers (column 8, lines 9-11; Figure 8).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hause, in view of Wolf, *Silicon Processing for the VLSI Era*, Vol. 4, Lattice Press (2002).

15. As to claim 4, Hause does not expressly disclose that the side-walls of the aperture are coated by means of a dielectric material having a low dielectric constant (k). However, Wolf teaches that low-k dielectric films are important in integrated circuit applications because they can significantly improve circuit performance characteristics (page 639). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a dielectric material having a low dielectric constant (k). One who is skilled in the art would be motivated to use a material that can significantly improve circuit performance characteristics.

16. As to claim 5, Hause does not expressly disclose that the dielectric material of the coating layer is chosen from among fluorous glass, glass deposited by spinning and silicon oxide containing carbon. Wolf teaches that silicon oxide containing carbon (or C-dope oxide (Si-O-C)) is a commonly used low-k material (page 646, Table 14-3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a dielectric material of the coating layer chosen from silicon oxide containing carbon. One who is skilled in the art would be motivated to use a

commonly used low-k material, known to possess the characteristics to be successfully used in an integrated circuit.

17. As to claim 6, Hause discloses that the window of the mask (108) registers with at least one active part of the substrate (102) (column 6, lines 7-14) (from Figure 3, the window in mask (108) overlies (102). Hause does not expressly disclose that said active part of the substrate (102) is exposed during the etching of the intermediate layer of material through the window of the mask (Figure 4). However, Hause discloses that (104) is silicon oxide (column 6, lines 15-18). Additionally, Wolf teaches that low-k dielectric films (i.e., $k < 3.9$ for silicon oxide) are important in integrated circuit applications because they can significantly improve circuit performance characteristics (page 639). Thus, there is a suggestion for exposing the active part of the substrate (102) during the etching of the intermediate layer of material through the window of the mask, because performing this step would reduce the volume of silicon oxide, replacing this material with the low-k dielectric side-walls, as in the combined teachings. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to expose the active part of the substrate during the etching of the intermediate layer of material through the window of the mask.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chang (U.S. Patent Appl. Pub. No. 2002/0137331) discloses forming sidewalls in an aperture to reduce its dimensions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC EBC
May 18, 2006

SHAMIM AHMED
PRIMARY EXAMINER